A 16-Channel 220 μW neural recording IC with embedded delta compression

Vahid Majidzadeh, Alexandre Schmid, and Yusuf Leblebici
Microelectronic Systems Laboratory (LSM), Swiss Federal Institute of Technology (EPFL), CH-1015 Lausanne
Email: vahid.majidzadeh@epfl.ch

***Abstract*— A 16-channel neural action potential recording IC suitable for large-scale integration with multi-electrode arrays (MEAs) is presented. A closed-loop gain of 60 dB in the action potential band is achieved by cascading differential gain-stages utilizing a novel CMFB circuit. An oversampling delta modulator (DM) is proposed to improve the noise efficiency factor (NEF) of the recording system. Moreover, in-site compression is achieved by converting the derivative of the neural signal. The DM employs a novel dynamic voltage comparator with a partial reset preamplifier, which enhances the mean time to failure of the modulator. The proposed architecture is fabricated in a 0.18 μm CMOS technology. The total power consumption for 16 channels is 220 μW from a 1.2 V power supply. The SNDR is measured at 28.3 dB and 35.9 dB at the modulator and demodulator outputs, respectively. The total integrated in-band input-referred noise including the quantization noise of the ADC is measured at 2.8 μV_{rms}, which corresponds to NEF=4.6 for the entire system.**

I. Introduction

Minimally invasive monitoring of the electrical activity of specific brain areas using implantable microsystems offers the promise of diagnosing brain diseases, as well as detecting and identifying neural patterns which are specific to a behavioral phenomenon. Neural pattern classification and recognition require simultaneous recording from a large number of neurons [1]. However, extensive recording $in-vivo$ demands complying with severe requirements. Low-power and low-noise operation, stable DC interface with sensors (microprobes), and small silicon area are the main design specifications of these recording systems.

The multichannel recording system in [2] use a single SAR ADC and a time-multiplexing technique to digitize the neural signals at the cost of losing some temporal information of the channels due to the scanning nature of the time-multiplexing technique. The optimum number of channels per ADC that minimizes the total power consumption of the system is presented in [3]. In [4], a dedicated incremental $\Delta\Sigma$ ADC is used to enhance the NEF. A compressive modulation scheme based on a double sampling analog memory and a switched-capacitor delta circuit is presented in [5] which enables reducing the dynamic range requirement of the ADC and the data rate. Finally, a very recent work presented in [6] uses DC coupling with sensor and active feedback to reduce the silicon area.

In this paper oversampling is used to improve the system NEF and reduce the silicon area. A single-bit continuous-time delta modulator acts as an ADC as well as an embedded delta compression module. Fully differential circuit implementation is accomplished by proposing a linear and large swing common-mode feedback (CMFB) circuit and a dynamic voltage comparator with partial reset preamplifier. The system speed and resolution are programmable and can also be used as a spike detection circuitry.

This paper is organized as follows. Section II describes the proposed system architecture. Section III presents the circuit implementation of the system. Measurement results of the system are presented in Section IV. Finally, Section V concludes the paper.

II. System architecture

Fig. 1 shows the architecture of the proposed 16-channel neural recording system, which includes amplification stages, a delta modulator ADC, a programmable bias generator enabling speed/resolution scalability, and IO buffers. A dedicated ADC is used in each channel to boost the SNR in the recording site and enhance the robustness to interferences. The input-referred noise of each channel should be smaller than the background noise of the neuron and electrode ($\approx 5\mu V_{rms}$), the area of each pixel should be smaller than 400μm$\times$400μm to be compatible with the pitch of the targeted commercial MEAs (Utah's MEA).

Oversampling is presented as a system-level solution to reduce the input-referred noise and the silicon area. The contribution of the oversampling ADC to the total system power consumption can be neglected, since the system is noise-limited and the power consumption is dominated by the low-noise analog front-end. A strong trade-off between noise and silicon area dictates circuit design specifications. According to the channel noise model shown in Fig. 2, the input-referred noise due to folding out of band circuit noise is reduced by limiting the bandwidth of the front-end gain-stage. However, bandwidth limitation of the front-end requires large on-chip capacitors due to the large transconductance of the stage. Since the stages following the front-end stage require smaller transconductances due to relaxed noise requirements, the bandwidth limitation is consequently performed at these stages. An optimization algorithm is developed to find the optimum allocation of the closed-loop gain and bandwidth of the different stages, as well as the optimum scaling factor for decoupling capacitors of cascaded stages which minimizes NEF and area, concurrently.

The delta modulator quantizes the temporal difference in the input signal, thus achieving compression of slow varying inputs. Using oversampling ratio (OSR), the maximum SNR for

978-1-4577-1470-2/11/$26.00 ©2011 IEEE

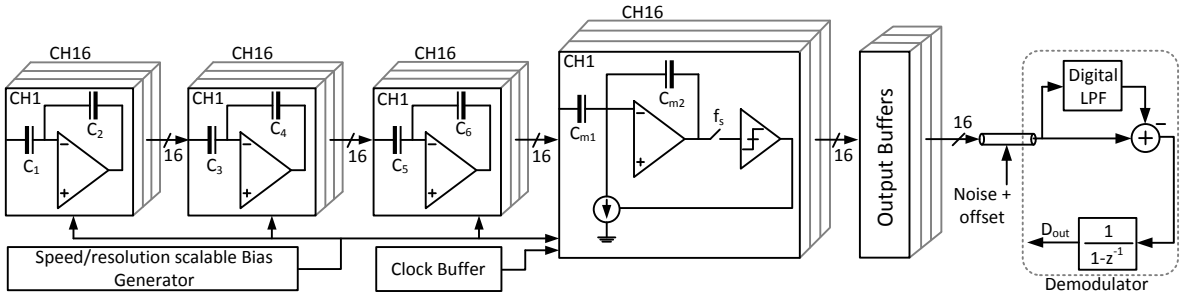

Fig. 1. Architecture of the 16-channel neural recording system and reconstruction circuit at the receiver.

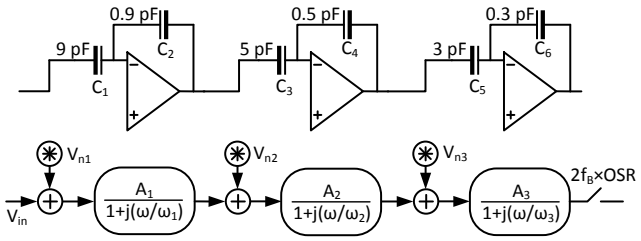

Fig. 2. Noise contribution of the different stages.

a single-tone input assuming the absence of slope-overloading effect is expressed:

$$SNR = -2.16 + 30log(OSR) \quad (1)$$

The single-bit oversampled digital output facilitates data logging from large number of channels, but increases the amount of generated raw data. Table I presents a comparison of data rates generated by a delta modulator and an equivalent Nyquist rate ADC for an identical effective number of bits (ENOB). The DM can be used as a spike detection circuitry for low OSR values where the penalty in data rate is negligible in comparison with a Nyquist rate ADC (N-ADC), even transmitting raw data. For fine-resolution recording, the difference in data rate is more pronounced, which can be mitigated either using an on-chip decimation filter or developing an energy efficient data transmission link such as impulse radio ultra wide band (IR-UWB).

The block diagram of the reconstruction circuit is shown in Fig. 1. The output of the modulator consist of the derivative of the input signal. A digital accumulator at receiver side serves as the reconstruction block. In order to avoid overflow of the accumulator, the DC offset of the channel is estimated and filtered out by the means of a low-pass filter. In this paper, reconstruction is performed by off-chip signal processing using Matlab.

III. Circuit Implementation

1) Gain Stage:

Fig. 3(a) shows the architecture of the gain stage. All three stages have an identical architecture however providing different bandwidths. Capacitive coupling allows rail-to-rail DC offset rejection at the sensor interface. Moreover, it isolates

TABLE I
Comparison between data rates of DM and N-ADC.

OSR	SNR (dB)	ENOB	DM (b/s)	N-ADC (b/s)
4	16	2.4	50 k	37.5 k
8	25	3.9	100 k	50 k
16	34	5.4	200 k	75 k
32	43	6.9	400 k	87.5 k

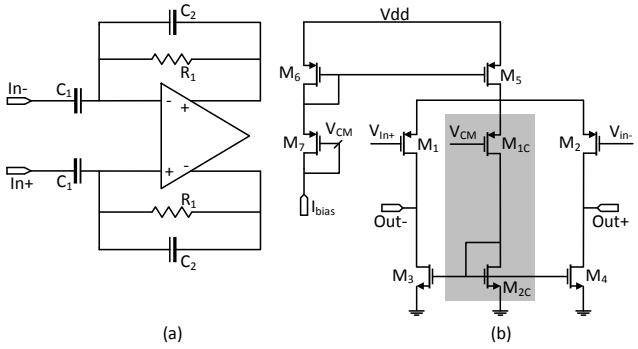

Fig. 3. (a) Capacitively coupled gain stage, and (b) circuit schematic with linear and high-swing CMFB circuit.

the common mode voltage of the different gain stages. The midband gain of the stage is determined by the capacitor ratio C_1/C_2. According to system-level optimization of the gain and bandwidth of the stages, midband gain of 20 dB at each stage is required. The high-pass cut-off frequency is determined by the time constant of the feedback devices R_1 and C_2. Large value resistors R_1 are realized by sub-threshold MOS devices.

Fig. 3(b) shows the circuit implementation of the OTA. A single-stage OTA enables meeting the 20 dB closed-loop midband gain requirement. The low-noise requirement, specially severe at the first stage, imposes the operation of the input devices M_{1-2} and the load devices M_{3-4} in weak and strong inversion regimes, respectively. The proposed CMFB circuit is composed of M_{1C} and M_{2C} and is shown in shaded box of Fig. 3(b). A small fraction of the bias current provided by M_5 is conveyed by M_{1C}. Any change in the output common-mode voltage is sensed by input devices M_{1-2} through the high value feedback resistors R_1, and is regulated by the shunt and current copy devices M_{1C} and M_{2C}, respectively.

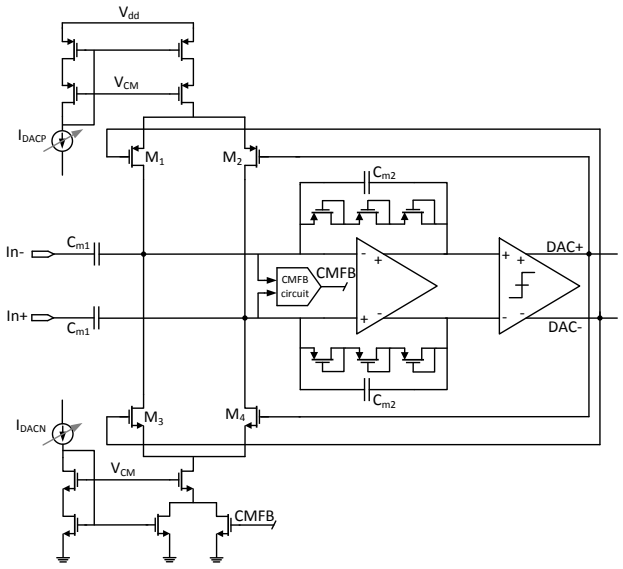

Fig. 4. Delta modulator with a single-bit current steering DAC.

2) ADC:

Figure 4 shows the architecture of the single-bit delta modulator ADC. Devices M_{1-4} along with the low-swing cascode current sources are used as a single-bit current steering DAC. The gain of the feedback DAC is determined by I_{DAC}/C_{m2} and is digitally programmable to accommodate different values of OSRs. A CMFB circuit is required at the output of the DAC to compensate for the mismatch between NMOS and PMOS current sources.

An operational transconductance amplifier (OTA) serves as a continuous-time gain stage for the signal path ($G = C_{m1}/C_{m2}$) and as a continuous-time integrator for feedback path signals DAC- and DAC+. High-level simulation results shows that 40 dB of DC gain in the OTA is required to preserve the SNR at OSR=32. A single-stage OTA identical to Fig. 3 is used. The DC feedback provided by sub-threshold devices is indispensable for CMFB operation. However, the limited impedance of these devices results in a lossy integrator. A small-signal resistance larger than 10 GΩ is required to preserve the SNR at OSR=32. Since the swing at the output of the gain stage is limited to a value corresponding to one V_{LSB} of the ADC, large resistance of 10 GΩ can easily be achieved by sub-threshold devices [2].

3) Voltage Comparator:

In conventional dynamic voltage comparator architectures [7], a reset device M_R is used to reset the state of the output latch during the pre-amplification phase. Thus, the gain of the preamplifier is determined by the ratio of the transconductance of the input devices M_{1-2} (g_{m1-2}) and the channel resistance of M_R. Hence, increasing the channel length of the reset device, a larger preamplifier gain can be achieved at the cost of the increased parasitic capacitance at the regenerative nodes. Consequently, a strong trade-off between preamplifier gain and regeneration time constant must be accounted for.

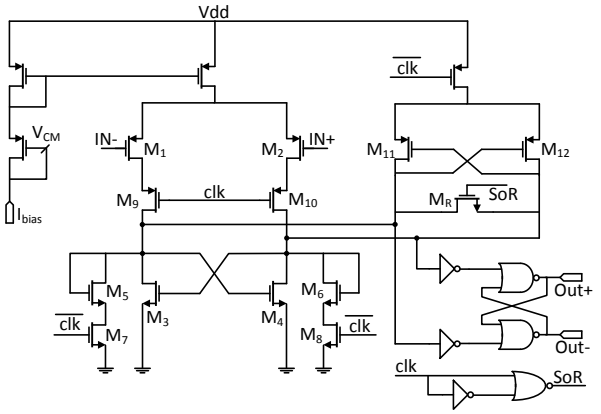

Fig. 5. Dynamic voltage comparator with partially reset preamplifier.

The proposed dynamic voltage comparator architecture which is shown in Fig. 5, the preamplifier stage is composed of M_{1-10} and the regenerative latch is composed of M_{11-12}. An SR latch is used at the output of the comparator, which preserves data for a full period of the clock. In this architecture, a minimum channel length device M_R is used to partially reset the latch at the beginning of the pre-amplification phase, which reduces the parasitic capacitance at regeneration node and reduces the regeneration time constant (τ). The partial reset phase is generated by a negative edge detector and the duration of the reset is controlled by the delay of the inverting element in the edge detector circuit. When the reset signal SoR is released at the gate of M_R, the gain of the preamplifier is expressed by:

$$A_p = \frac{g_{m1}}{g_{m5} - g_{m3}} \tag{2}$$

A larger A_p is achieved by making $g_{m5} \approx g_{m3}$. Moreover, simulation results shows that the gain has less sensitivity to process variation in comparison with conventional architectures. The metastability of the comparator is an important design metric in this architecture. Wrong decision of the comparator will be accumulated in the demodulator and results in a constant error when reconstructed, until the next error takes place. The mean value of errors approaches zero assuming that the probabilities of erroneous detection 0 and 1 are the same and equal to 50%. The probability of error is characterized in terms of mean time to failure (MTF):

$$MTF = \frac{K \cdot A_p}{f_s \cdot V_{DD}} \cdot exp\left(\frac{A_0 - 1}{2 f_s \cdot \tau}\right) \tag{3}$$

where f_s is the sampling frequency, K is the signal swing at the input of the comparator, A_p is the preamplifier gain, A_0 refers to the latch gain, and τ stands for the time constant of regeneration. Consequently, improving the trade-off between A_p and τ in the proposed architecture improves the MTF and BER.

IV. Measurement Results

The proposed action potential recording system is fabricated in a 1P6M 0.18 μm CMOS technology. Figure 6 shows the

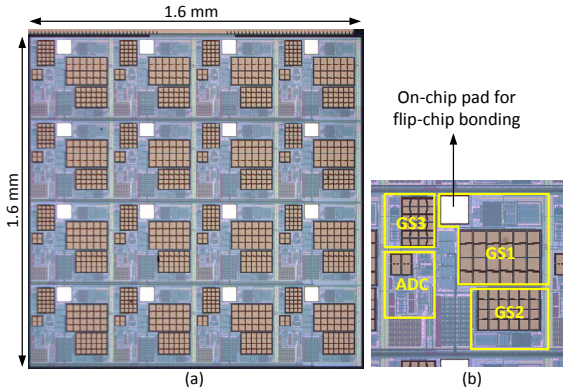

Fig. 6. (a) Die photograph of the 16-channel neural recording system (b) close-up die photograph of a single channel.

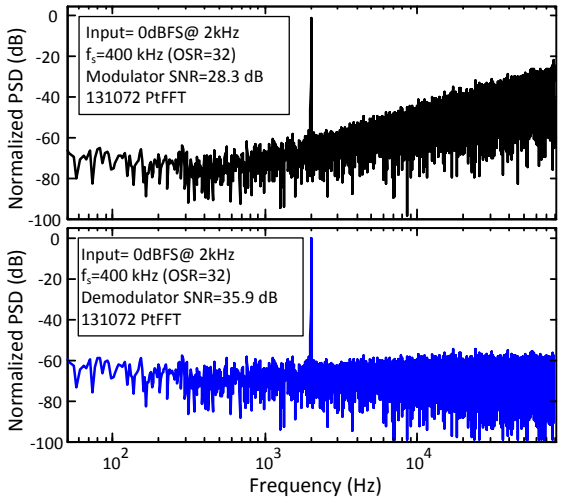

Fig. 7. (top) Power spectral density of an active channel in the modulator, (bottom) power spectral density of an active channel in the demodulator.

die photograph of the active silicon area for 16 channels. The total occupied silicon area is 1.6mm×1.6mm, which results in an effective silicon area of 0.16 mm^2 for each recording site and is compatible with the University of Utah's MEA, which has an inter-electrode pitch of 400 μm. On-chip pads will be used for flip-chip bonding.

Figure 7(top) shows the measured power spectral density (PSD) of an active channel when stimulated with a single tone sinusoid at 2 kHz, 500 μV_{p-p} amplitude, and sampled at 400 kHz. The SNDR is measured equal to 28.3 dB at the output of the modulator. Demodulation is done by off-chip signal processing in Matlab based on the architecture shown in Fig. 1. The PSD is shown in Fig. 7(bottom) with a SNDR measured equal to 35.9 dB, which presents 7.6 dB of compression for a single tone input signal.

The total current consumption of the chip including the data buffers is 183.2 μA, which corresponds to 11.5 μA of current consumption for a single channel from a 1.2 V power supply. The front-end low-noise amplifier consumes 73% of the total power consumption due to the low noise requirement

TABLE II
SUMMARY OF PERFORMANCE AND COMPARISON.

Parameter	[4]	[6]	this work
Technology (CMOS)	0.5μm	65nm	0.18μm
Supply voltage	3.3 V	0.5 V	1.2 V
Supply current/Ch	34 μA	10.1 μA	11.5 μA
Gain	39.6 dB	32 dB	60 dB
Bandwidth (kHz)	8.2	10	6.25
Input-referred noise	1.94 μV_{rms}	4.9 μV_{rms}	2.8 μV_{rms}
System NEF	-	5.99	4.6
Offset rejection	rail-to-rail	$\pm$ 50mV	rail-to-rail
Area/Ch (mm^2)	0.56	0.013	0.16

and the ADC only consumes 1.3 μW at maximum OSR equal to 32. The total integrated input-referred in-band noise, including the quantization noise of the ADC is 2.8 μV_{rms}, which corresponds to a NEF of 4.6 for the total system. Table II shows the summary of performance and comparison with the most recent state-of-the art published works. The system in [6] uses an open-loop amplifier and large gain variation is expected in a multi channel recording system. The input-referred noise reported in [4] only includes the front-end amplifier and the system NEF is not available.

V. CONCLUSION

A 16-channel neural recording systems is presented. The optimum gain and bandwidth allocation of the cascaded amplifiers and the usage of a novel differential amplifier results in a power efficient differential implementation of the system. The oversampling delta modulator not only improves the system level NEF, but also provides in-site compression due to slow varying input signal. The partial reset preamplifier which is proposed at the voltage comparator, improves the MTF and bit error rate of the modulator/demodulator link, respectively.

VI. ACKNOWLEDGMENT

The authors acknowledge the support of the Swiss NSF under project 200020-122082, and the support of Hossein Afshari and Berkeley Wireless Research Center in measurements.

REFERENCES

[1] J. Wessberg, et.al, "Real-time rediction of hand trajectory by ensembles of cortical neurons in primates," *Nature*, vol. 408, pp. 361-365, Nov. 2000.

[2] R. R. Harrison, et.al,"A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123-133, June. 2007.

[3] M. S. Chae, W. Liu, and M. Sivaprakasam,"Design optimization for integrated neural recording systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1931-1939, Sept. 2008.

[4] M. Mollazadeh, K. Murari, G. Cauwenberghs, N. Thakor,"Micropower CMOS Integrated Low-Noise Amplification, Filtering, and Digitization of Multimodal Neuropotentials," *IEEE Trans. Biomedical Circuits Syst*, vol. 3, no. 1, pp. 1-10, Feb. 2009.

[5] J. N. Y. Aziz, et.al,"256-Channel Neural Recording and Delta Compression Microsystem With 3D Electrodes," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 995-1005, Mar. 2009.

[6] R. Muller, S. Gambini, and J. Rabaey,"A 0.013mm^2 5μW DC-DC-coupled neural signal acquisition IC with 0.5V supply," *ISSCC Dig. Tech. Papers*, pp. 302-303, Feb 2011.

[7] B. Razavi,"Principles of Data Conversion System Design," *IEEE press*, 1995.